REMARKS

The application has been reviewed in light of the non-final Office Action dated December 20, 2007. Claims 19, 20 and 22-38 were pending. By this Amendment, claims 19, 22 and 31 have been amended to clarify the claimed subject matter thereof, and new claims 39 and 40 have been added. Accordingly, claims 19, 20 and 22-40 are now pending, with claims 19, 22 and 31 being in independent form.

Claims 22 and 31 were rejected under 35 U.S.C. § 102(e) as purportedly anticipated by U.S. Patent No. 6,944,717 to Yoneyama et al. Claims 22-24 and 30-33 were rejected under 35 U.S.C. § 103(a) as purportedly unpatentable over Kasebayashi in view of U.S. Patent No. 6,799,242 to Tsuda et al. and U.S. Patent No. 6,799,242 to Tsuda et al. Claims 25, 26, 29 and 34-36 were rejected under 35 U.S.C. § 103(a) as purportedly unpatentable over Kasebayashi in view of Tsuda and further in view of U.S. Patent No. 6,470,439 to Yamada et al. Claims 27-28 and 37-38 were rejected under 35 U.S.C. § 103(a) as purportedly unpatentable over Kasebayashi in view of Tsuda and Yamada and further in view of U.S. Patent No. 6,502,159 to Chuang. Claims 19 and 20 were rejected under 35 U.S.C. § 103(a) as purportedly unpatentable over Kasebayashi in view of Tsuda and further in view of U.S. Patent No. 6,631,469 to Silvester.

Applicant respectfully submits that independent claims 19, 22 and 31 are patentable over the cited art, for at least the following reasons.

The present application relates to an improved approach devised by applicant for data transfer between an optical disk drive apparatus with a host computer.

Yoneyama, as understood by Applicant, proposes an approach for controlling and storing data in a cache buffer for reading and writing data from and to a hard disk drive, wherein the cache buffer includes a plurality of memory cells organized into pages (that is, the cache buffer

operates as a page cache).

Figure 2 of Yoneyama, which proposes a structure of a hard disk drive 18 having such a cache buffer 32, and Fig. 1, which illustrates a computer system which includes such a hard disk drive 18, are reproduced below:

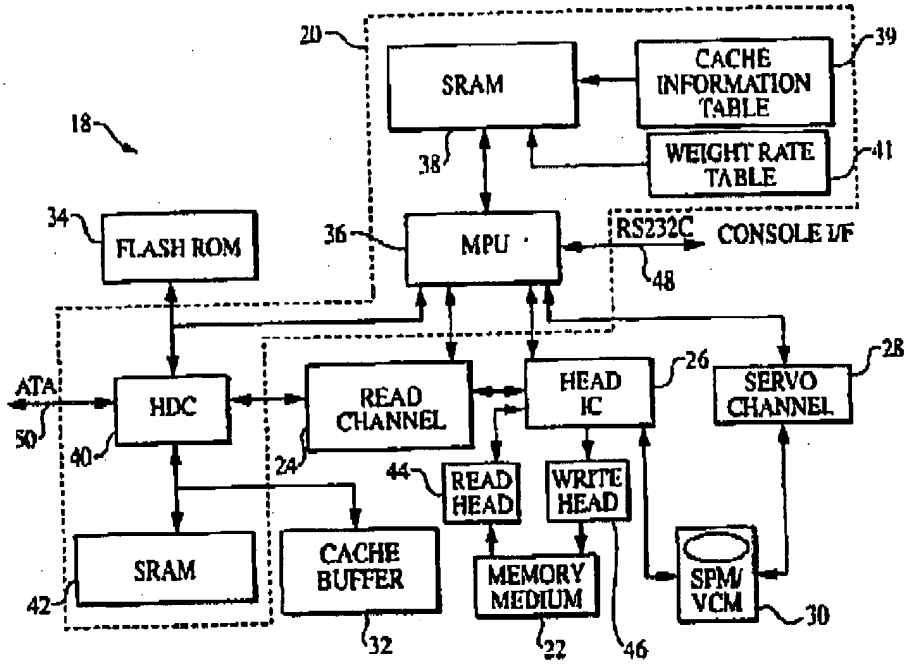


FIG. 2

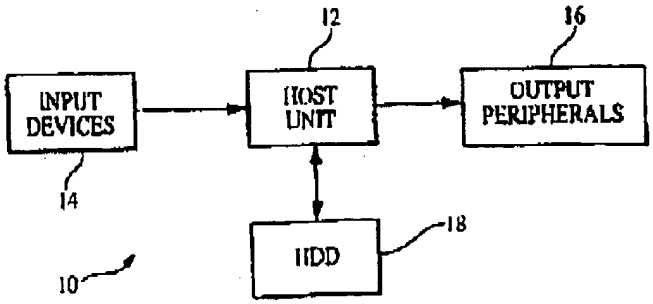


FIG. 1

The Office Action apparently equates elements 18, 39 and 22 shown in Fig. 2 of Yoneyama with the "optical disk drive mechanism", "first memory" and "second memory" of claim 22 of the present application.

However, as plainly evident in Fig. 2 of Yoneyama, medium 22 in Yoneyama is the hard disk storage medium in the hard disk drive 18 proposed by Yoneyama (see read head 44 and write head 46 which are coupled to read data from and write data to hard disk medium 22, as shown in Fig. 2 of Yoneyama). Therefore, assuming *arguendo* that the hard disk drive 18 can be aptly equated to the optical disk drive mechanism of claim 22 of the present application, then medium 22 would correspond to an optical disk medium but NOT to the "***second memory configured to store second information***, received by the second memory in association with the first information stored in the first memory and ***corresponding to the data read by the optical disk drive mechanism from the optical disk medium*** and to be transferred from the optical disk drive apparatus to the host computer, to be written into the specified registers at the specific addresses indicated by the first information stored in the first memory" (claim 22 of the present application).

Further, it is noted that Yoneyama, column 9, lines 10-20, corresponds to a step in the process proposed by (and shown in Fig. 7 of) Yoneyama for writing data from the host to the hard disk drive medium, and has nothing to do with performing an information writing operation in connection with the data read by the optical disk drive mechanism from the optical disk medium and to be transferred from the optical disk drive apparatus to the host computer (claim 22 of the present application).

Applicant submits that Yoneyama simply does not disclose or suggest the claimed subject matter of claim 22 of the present application, and independent claim 31 is patentable over

Yoneyama for at least similar reasons.

Kasebayashi, as understood by Applicant, proposes a magnetic disk drive apparatus including a buffer 11 having an area for storing burst data and another area for storing data in connection with write and read commands.

The Office Action equates buffer 11 and address storage 12 shown in Figure 3 (reproduced below) of Kasebayashi to the "register circuit" and "first memory" of claim 22 of the present application.

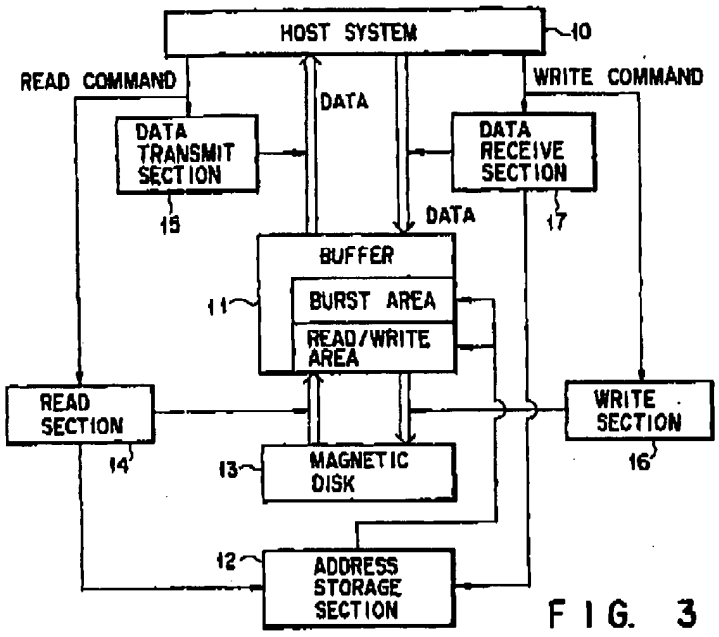


FIG. 3

In addition, the Office Action equates read unit 14 shown in Figure 3 of Kasebayashi to (i) a second memory configured to store second information, received by the second memory in association with the first information stored in the first memory and corresponding to the data read by the optical disk drive mechanism from the optical disk medium and to be transferred from the optical disk drive apparatus to the host computer, to be written into the specified registers at the specific addresses indicated by the first information stored in the first memory,

and (ii) a control circuit configured to perform an information writing operation for writing the first information and the second information into the first memory and the second memory, respectively, in chronological order of accesses executed, in connection with the data read by the optical disk drive mechanism from the optical disk medium and to be transferred from the optical disk drive apparatus to the host computer.

It is contended in the Office Action that "the read unit 14 actively reading data from magnetic disk 13 and separately writing the data to buffer 11 [using two distinct steps] would indicate that internal memory is necessarily required". It is also contended in the Office Action that "it is understood that the read unit 14 comprises of both a memory and a control circuit since both functions are performed as disclosed in Kasebayashi."

Applicant traverses the rejection and such contentions in the Office Action.

One of ordinary skill in the art considering Kasebayashi as a whole, including Figure 3 therein, would have understood that read unit 14 has a control function but not a storage function (that is, storage of data read from disk 13). The function of storing data read from disk 13 rests entirely with buffer 11.

When Kasebayashi states that the read unit 14 reads data required by the host system from the disk 13, one skilled in the art would undisputably understand such statement to mean that the read unit controls the operation to read the data from the disk 13 and write the data to the buffer 11.

One skilled in the art would have expected to find an arrow from disk 13 to read unit 14 in Fig. 3 of Kasebayashi, if Kasebayashi were proposing that data read by the read unit 14 is stored, even temporarily, in read unit 14. Such arrow is NOT present in Fig. 3 of Kasebayashi.

Further, the data read from the disk 13 is destined to be in buffer 11. What (if any)

purpose would there be to store such data, even temporarily, in read unit 14 before writing to buffer 11? ANSWER: one skilled in the art would conclude that there is no such purpose and would not have understood Kasebayashi to be proposing that the read unit 14 stores the data read from the disk 13.

The other cited references, as discussed in the record, do not cure the above-mentioned deficiencies of Kasebayashi.

The cited art, when considered along with the common sense and common knowledge of one skilled in the art, simply does not render obvious an optical disk drive apparatus comprising a communications interface apparatus comprising a register circuit, a first memory, a second memory and a control circuit, wherein (i) the register circuit includes a plurality of registers configured to store data read by said optical disk drive mechanism from said optical disk medium and to be transferred from the optical disk drive apparatus to a host computer, and (ii) the second memory stores second information, received by said second memory in association with the first information stored in the first memory and corresponding to said data read by said optical disk drive mechanism from said optical disk medium and to be transferred from the optical disk drive apparatus to said host computer, to be written into the specified registers at the specific addresses indicated by the first information stored in the first memory, as provided by the subject matter of claim 22 of the present application.

Independent claim 31 is patentably distinct from the cited art for at least similar reasons.

Accordingly, Applicant respectfully submits that independent claims 22 and 31, and the claims depending therefrom, are patentable over the cited art.

Regarding claim 19 of the present application, Kasebayashi, as acknowledged in the Office Action, does not disclose or suggest an apparatus including a clock generator which

generates a clock signal with which a data processor performs a predetermined data processing operation to data received through an input terminal, and an operation mode changer which controls the clock generator to reduce a frequency of the clock signal to a non-zero value smaller than a predetermined value to change an operation mode from a regular operation mode to a low power consumption mode.

Tsuda, as understood by Applicant, proposes an optical disc player apparatus that enters a sleep mode when it is inactive for a predetermined time.

The Office Action cites Tsuda column 7 line 56 –column 8 line 10 (reproduced below):

> Entry into the sleep mode will now be described. When a sleep command is issued from the host computer to the host interface 13, it is transferred via the microcomputer interface 233 to the control microcomputer 244, which responds by delivering a TOC transfer command to the memory control circuit 232 via the microcomputer interface 233. On the basis of the first address and the size data stored in the address register 230, the memory control circuit 232 reads the TOC data from the buffer RAM 7, and transfers it to the microcomputer interface 233, where a part of the TOC data is temporarily stored in a register (not shown). The memory control circuit 61 reads the TOC data stored in the register of the microcomputer interface 233, and writes it to the SRAM 56 in a sequential manner beginning with the first address. A succeeding portion of the TOC data continues to be written to a storage region of the SDRAM 56 for which the write operation has been completed. After the write operation of the TOC data into the SDRAM 56 is completed, ***the control microcomputer 244 delivers a stop command to the clock generator circuit 62, which then stops to generating the clock signal, thus entering the sleep mode***.

It is contended in the Office Action that "The clock generator producing no clock signals is equivalent to 'reducing a frequency of the clock signal', since the resulting clock frequency is less than the frequency of the clock in the normal operational mode (i.e., the clock frequency is reduced to zero)."

However, Tsuda does not disclose or suggest reducing a frequency of the clock signal to a ***non-zero*** value smaller than a predetermined value to change an operation mode from a regular operation mode to a low power consumption mode.

Silvester, as understood by Applicant, proposes a computer system having a sleep mode, and in the sleep mode, a wakeup alarm is triggered in the computer system according to a user-specified periodic interval, and in response to the wakeup alarm, the computer system automatically exits the sleep mode and enters a wake mode, and then automatically exchanges data, such as email, with a host and thereafter returns to the sleep mode.

However, Silvester, like Tsuda and the other cited references, do not disclose or suggest reducing a frequency of the clock signal to a ***non-zero*** value smaller than a predetermined value to change an operation mode from a regular operation mode to a low power consumption mode, according to the subject matter of claim 19 of the present application.

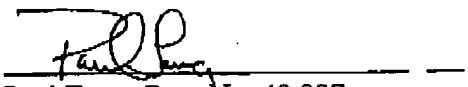
Accordingly, applicant submits that independent claim 19 and the claims depending therefrom are patentable over the cited art.

In view of the remarks hereinabove, Applicant submits that the application is now in condition for allowance, and earnestly solicits the allowance of the application.

If a petition for an extension of time is required to make this response timely, this paper should be considered to be such a petition. The Patent Office is hereby authorized to charge any required fees, and credit any overpayment, to our Deposit Account No. 03-3125.

If a telephone interview could advance the prosecution of this application, the Examiner is respectfully requested to call the undersigned attorney.

Respectfully submitted,



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